

TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

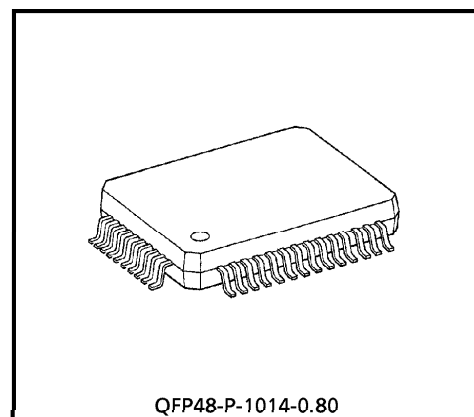
TA2065F

CD FOCUS TRACKING SERVO LSI

The TA2065F is a 3-beam type PUH compatible focus tracking servo LSI to be used in the CD player system. In combination with a CMOS single chip processor TC9236AF/TC9263AF/TC9283F/TC9284AF, a CD player system can be composed very simply.

FEATURES

- Built-in RF amp, focus error amp, and tracking error amp.
- Built-in focus tracking servo amp.
- Built-in phase compensation amp and LPF amp.
- Built-in ALPC amp.
- Connections between PUH and power driver IC for motor driver allow simplified structuring of CD player system.
- Double speed operation is possible.
- Low voltage operation is possible. (3.5~5.5V)

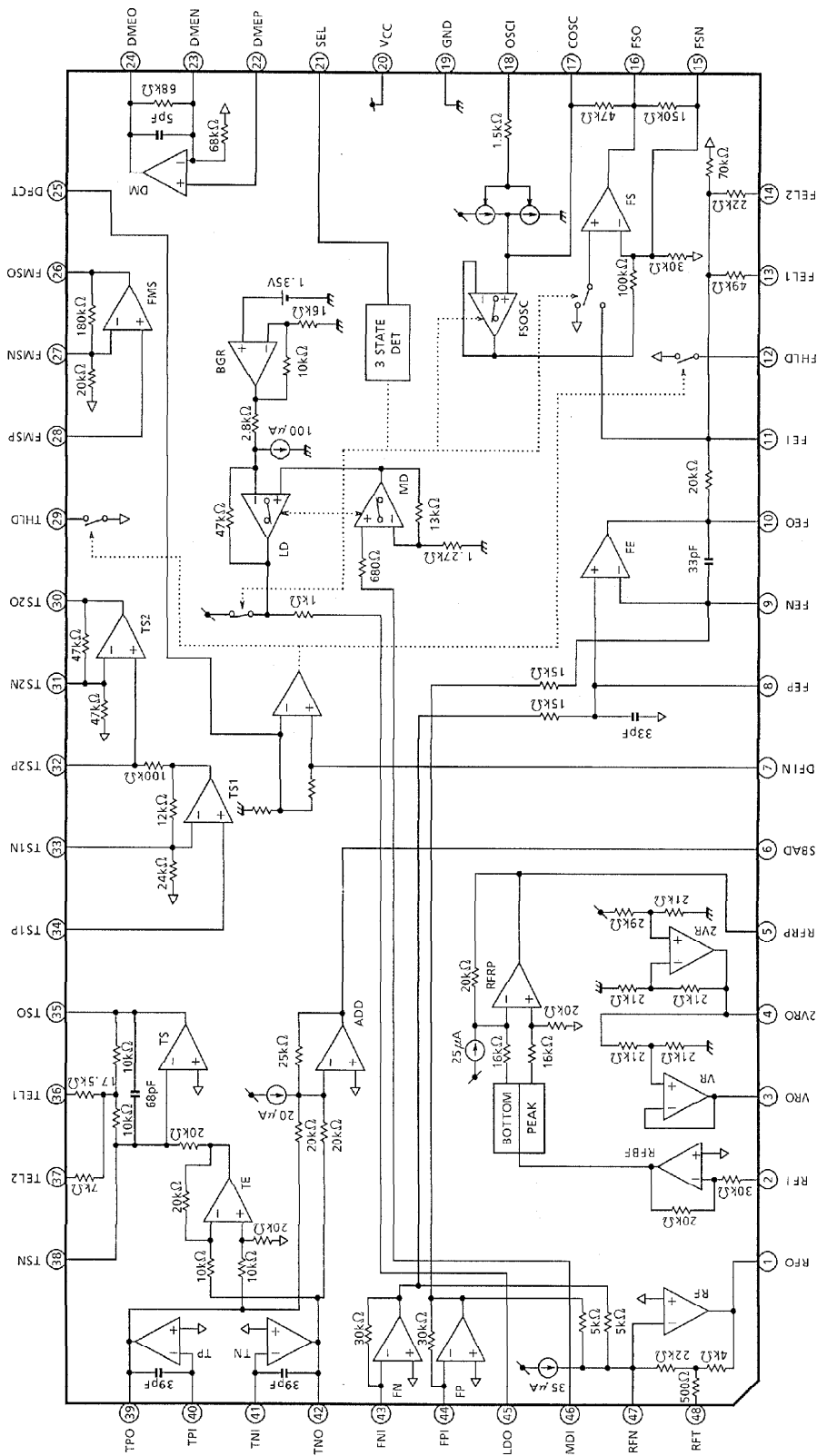


Weight : 0.83g (Typ.)

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BLOCK DIAGRAM



TA2065F-2

PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	RFO	O	RF amp (RF AMP) output terminal.	
2	RFI	I	RF ripple signal generating circuit input terminal.	Connected to RFO through C.
3	VRO	O	VR amp output terminal.	
4	2VRO	O	2VR amp output terminal.	
5	RFRP	O	RF ripple signal output terminal.	
6	SBAD	O	Defects detection signal output terminal.	
7	DFIN	I	Defect detecting comparator positive phase input terminal.	
8	FEP	I	Focus error balance adjusting input terminal.	Adjusting semi-fixed resistor is connected.
9	FEN	I	Focus error amp (FE AMP) negative phase input terminal.	
10	FEO	O	Focus error amp (FE AMP) output terminal.	
11	FEI	I	Focus output amp (FS AMP) positive phase input terminal.	
12	FHLD	I	Hold switch terminal for defect.	
13	FEL1	I	Focus gain adjusting terminal.	
14	FEL2	I	Focus gain adjusting terminal.	
15	FSN	I	Focus output amp (FS AMP) negative phase input terminal.	
16	FSO	O	Focus output amp (FS AMP) output terminal.	
17	COSC	O	Focus search signal generating capacitor connecting terminal.	
18	OSCI	I	Focus search signal generating built-in current source control input terminal.	
19	GND	—	Ground terminal.	
20	VCC	—	Power source terminal.	
21	SEL	I	Analog switch control signal input terminal.	
22	DMEP	I	Disc motor amp (DM AMP) positive phase input terminal.	
23	DMEN	I	Disc motor amp (DM AMP) negative phase input terminal.	
24	DMEO	O	Disc motor amp (DM AMP) output terminal.	
25	DFCT	I	Defect detecting comparator negative phase input terminal.	
26	FMSO	O	Feed motor output amp (FMS AMP) output terminal.	
27	FMSN	I	Feed motor output amp (FMS AMP) negative phase input terminal.	

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
28	FMSP	I	Feed motor output amp (FMS AMP) positive phase input terminal.	
29	THLD	I	Hold switch terminal for defect.	
30	TS2O	O	Tracking servo amp 2 (TS2 AMP) output terminal.	
31	TS2N	I	Tracking servo amp 2 (TS2 AMP) negative phase input terminal.	
32	TS2P	I	Tracking servo amp 2 (TS2 AMP) positive phase input terminal.	
33	TS1N	I	Tracking servo amp 1 (TS1 AMP) negative phase input terminal.	
34	TS1P	I	Tracking servo amp 1 (TS1 AMP) positive phase input terminal.	
35	TSO	O	Tracking output amp (TS AMP) output terminal.	
36	TEL1	I	Tracking gain adjusting terminal.	
37	TEL2	I	Tracking gain adjusting terminal.	
38	TSN	I	Tracking output amp (TS AMP) negative phase input terminal.	
39	TPO	O	Sub-beam I-V amp output terminal.	Connected to TPI through adjusting feedback resistor.
40	TPI	I	Sub-beam I-V amp input terminal.	Connected to PIN diode E.
41	TNI	I	Sub-beam I-V amp input terminal.	Connected to PIN diode F.
42	TNO	O	Sub-beam I-V amp output terminal.	Connected to TNI through adjusting feedback resistor.
43	FNI	I	Main-beam I-V amp input terminal.	Connected to PIN diode A + C.
44	FPI	I	Main-beam I-V amp input terminal.	Connected to PIN diode B + D.
45	LDO	O	Laser diode amp output terminal.	Connected to laser diode circuit.
46	MDI	I	Monitor photo diode amp input terminal.	Connected to monitor photo diode.
47	RFN	I	RF amp negative phase input terminal.	
48	RFT	I	RF amp peaking terminal.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{CC}	-0.3~12.0	V
Power Dissipation	P _D	890 (*)	mW
Operating Temperature	T _{opr}	-35~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(*) Derated above 25°C in the proportion of 7.1mW/°C.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Source	Power Supply Voltage	V _{CC}	—		3.5	5.0	5.5	V
	Power Supply Current	I _{CC}	—	SEL = HiZ	14.0	24.0	32.0	mA
Reference Power Supply 2VREF [4]	Reference Voltage	2VR	—		4.0	4.2	4.4	V
	Output Current	I _{OH2}	—	ΔV = -0.1V	5.0	—	—	mA
	Input Current	I _{OL2}	—	ΔV = +0.1V	0.2	—	—	mA
Reference Power Supply VREF [3]	Reference Voltage	VR	—		2.0	2.1	2.2	V
	Reference Voltage Limit	ΔVR	—	2 × VR / 2VR - 1	-3.0	0.0	3.0	%
	Output Current	I _{OH1}	—	ΔV = -0.1V	5.0	—	—	mA
	Input Current	I _{OL1}	—	ΔV = +0.1V	5.0	—	—	mA
FS FEI [11] →FSO [16]	Voltage Gain	G _V	—	f = 1kHz	5.4	6.0	6.6	V/V
	Input Operating Voltage	V _I	—		1.0	—	4.4	V
	Output Offset Voltage	V _{OS}	—	VR reference	-12	—	12	mV
	Total Harmonic Distortion	THD	—	f = 1kHz, V _{FSO} = 1V _{p-p}	—	-65	—	dB
	Upper Limit Output Voltage	V _{OH}	—	GND reference	3.8	—	—	V
	Lower Limit Output Voltage	V _{OL}	—	GND reference	—	—	0.5	V
OSC OSCI [18] →FSO [16]	Output Amplitude	V _O	—	R (OSCI) = 15kΩ f (OSCI) = 0.5Hz (CMOS level)	—	1.6	—	V _{p-p}
	Output Offset Voltage	V _{OS}	—	OSCI = HiZ	-50	—	50	mV
	Output Switch Isolation	V _{ISO}	—	f _{COSC} = 1kHz, SEL = H	—	-65	—	dB

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
APC MDI [46] →LDO [45]	Voltage Gain	G_V	—	$f = 1\text{kHz}$	170	200	230	V/V	
	Operation Reference Voltage	V_{MDI}	—	$V_{LDO} = 3.5\text{V}$	170	178	192	mV	
	LD Off Voltage	V_{LDOF}	—	V_{CC} reference, SEL = L	-0.7	—	—	V	
	Input Bias Current	I_I	—		-200	—	200	nA	
FE FNI (FPI) [43] (44) →FEO [10]	Transfer Resistance	R_T	—	$f = 1\text{kHz}$ $FEN - FEO = 68\text{k}\Omega$ $FEP - VR = 68\text{k}\Omega$	122	136	150	$\text{k}\Omega$	
	Gain Balance	GB	—	$f = 1\text{kHz}$ $FEN - FEO = 68\text{k}\Omega$ $FEP - VR = 68\text{k}\Omega$	-1.0	—	1.0	dB	
	Frequency Characteristic	f_c	—		50	70	90	kHz	
	Output Offset Voltage	V_{OS}	—		-50	—	50	mV	
	Total Harmonic Distortion	THD	—	$f = 1\text{kHz}$, $V_{FEO} = 1.6\text{V}_{p-p}$	—	-65	—	dB	
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V	
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V	
	Permissive Load Resistance	R_{LM}	—		10	—	—	$\text{k}\Omega$	
FE FEO [10] →FEI [11]	Voltage Gain 1	G_{V1}	—	$f = 1\text{kHz}$	FEL1 = FEL2 = VR	0.36	0.38	0.40	V/V
	Voltage Gain 2	G_{V2}			FEL1 = HiZ, FEL2 = VR	0.44	0.46	0.48	
	Voltage Gain 3	G_{V3}			FEL1 = VR, FEL2 = HiZ	0.56	0.59	0.62	
	Voltage Gain 4	G_{V4}			FEL1 = FEL2 = HiZ	0.74	0.78	0.82	
RF FPI (FNI) [44] (43) →RFO [1]	Transfer Resistance	R_T	—	$f = 100\text{kHz}$	125	156	187	$\text{k}\Omega$	
	Frequency Characteristic	f_c	—		—	3.0	—	MHz	
	Output Slew Rate	SR	—	$C_{RFO} = 20\text{pF}$	—	20	—	$\text{V}/\mu\text{s}$	
	Total Harmonic Distortion	THD	—	$f = 100\text{kHz}$, $V_{RF} = 1.4\text{V}_{p-p}$	—	-50	—	dB	
	Operation Reference Voltage	V_{OPR}	—	VR reference	-1.21	-1.10	-0.99	V	

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
RF FPI (FNI) [44] (43) →RFO [1]	Upper Limit Output Voltage	V _{OH}	—	GND reference	3.6	—	—	V	
	Lower Limit Output Voltage	V _{OL}	—	GND reference	—	—	0.7	V	
	Permissive Load Resistance	R _{LM}	—		10	—	—	kΩ	
RFRP RFI [2] →RFRP [5]	Voltage Gain	G _V	—	f = 1kHz	0.75	0.83	0.92	V/V	
	Input Operating Voltage	V _I	—	GND reference	1.0	—	3.4	V	
	Peak Detecting Frequency Characteristic	f _{CPD}	—		—	80	—	kHz	
	Bottom Detecting Frequency Characteristic	f _{CBD}	—		—	80	—	kHz	
	Operation Reference Voltage 1	V _{OPR1}	—	VR reference No signal	-0.55	-0.50	-0.45	V	
	Operation Reference Voltage 2	V _{OPR2}	—	f = 700kHz, 1.4V _{p-p} VR reference	0.50	0.55	0.60	V	
	Permissive Load Resistance	R _{LM}	—		10	—	—	kΩ	
TS TPI (TNI) [40] (41) →TSO [35]	Transfer Resistance 1	R _{T1}	—	R _{NF} (TP, TN) = 180kΩ	TEL1 = TEL2 = HiZ	324	360	396	kΩ
	Transfer Resistance 2	R _{T2}			TEL1 = VR, TEL2 = HiZ	417	463	509	
	Transfer Resistance 3	R _{T3}			TEL1 = HiZ, TEL2 = VR	555	617	679	
	Transfer Resistance 4	R _{T4}			TEL1 = TEL2 = VR	648	720	792	
	Gain Balance	GB	—			-1.0	—	1.0	dB
	Frequency Characteristic	f _c	—			—	22	—	kHz
	Output Slew Rate	SR	—	C _{TSO} = 0.022μF		—	500	—	V/ms
	Output Offset Voltage	V _{OS}	—	VR reference		-50	—	50	mV

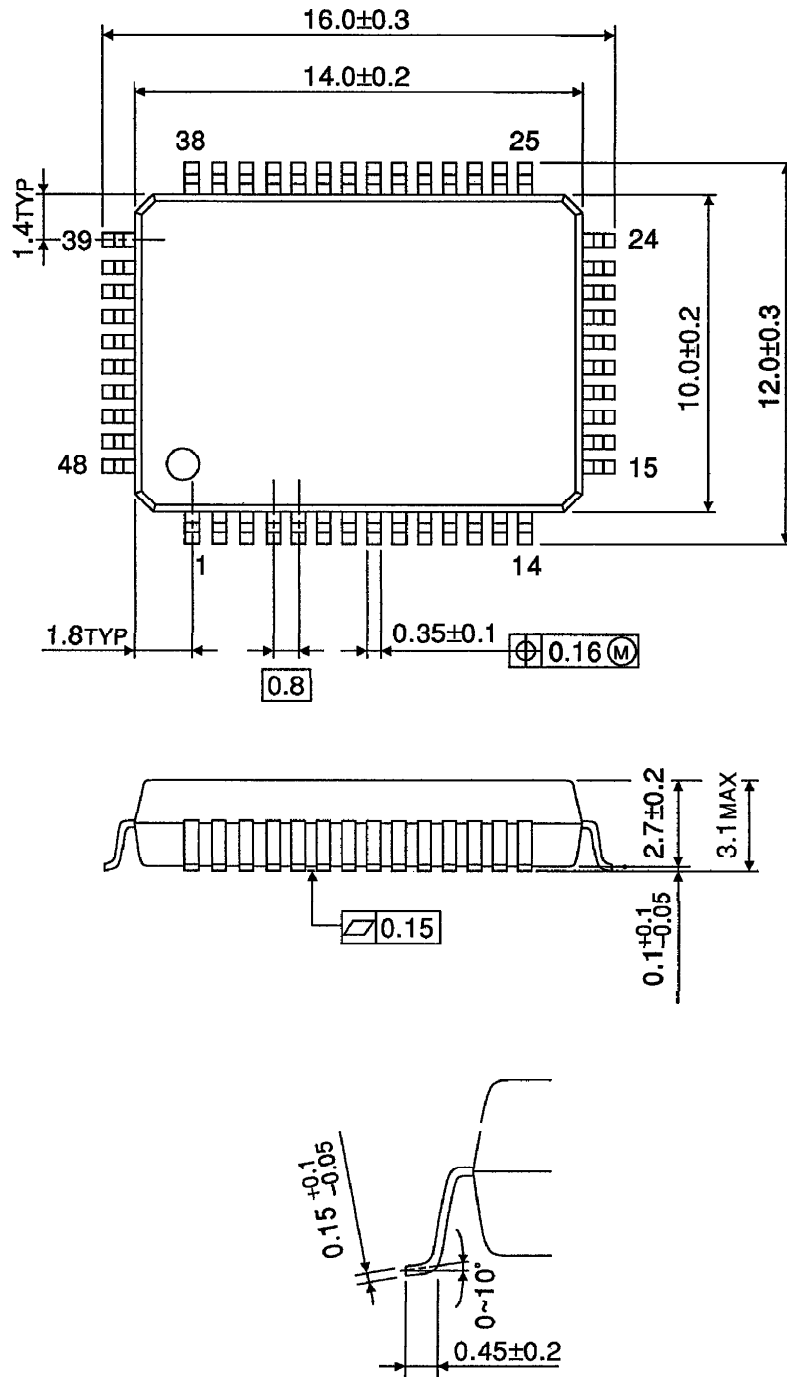
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
TS TPI (TNI) [40] (41) →TSO [35]	Total Harmonic Distortion	THD	—	f = 1kHz, $V_{TS} = 0.8V_{p-p}$	—	- 65	—	dB	
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V	
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V	
	Permissive Load Resistance	R_{LM}	—		10	—	—	k Ω	
SBAD TPI (TNI) [40] (41) →SBAD [6]	Transfer Resistance	R_T	—	f = 1kHz $R_{NF} (TP, TN) = 180k\Omega$	203	225	248	k Ω	
	Frequency Characteristic	f_c	—		—	22	—	kHz	
	Total Harmonic Distortion	THD	—	f = 1kHz $V_{SBAD} = 1.0V_{p-p}$	—	- 65	—	dB	
	Operation Reference Voltage	V_{OPR}	—	VR reference	-0.55	-0.50	-0.45	V	
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V	
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V	
	Permissive Load Resistance	R_{LM}	—		10	—	—	k Ω	
TS1 TS1P [34] →TS2P [32]	Voltage Gain 1	G_{V1}	—	f = 1kHz	TS2P = OPEN	1.43	1.50	1.58	V/V
	Voltage Gain 2	G_{V2}			TS2P - VR = 18k Ω	0.18	0.23	0.27	
	Input Operating Voltage	V_I	—		1.0	—	4.4	V	
	Output Offset Voltage	V_{OS}	—		- 10	—	10	mV	
	Total Harmonic Distortion	THD	—	f = 1kHz, $V_{TS2P} = 1V_{p-p}$	—	- 65	—	dB	
	Upper Limit Output Voltage	V_{OH}	—		3.8	—	—	V	
	Lower Limit Output Voltage	V_{OL}	—		—	—	0.5	V	
	Input Bias Current	I_I	—		- 100	—	100	nA	

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
TS2 TS2P (TS2N) [32] (31) →TS2O [30]	Voltage Gain	G_V	—	$f = 1\text{kHz}$	1.9	2.0	2.1	V/V
	Input Operating Voltage	V_I	—	GND reference	1.0	—	4.4	V
	Output Offset Voltage	V_{OS}	—	VR reference	-10	—	10	mV
	Total Harmonic Distortion	THD	—	$f = 1\text{kHz}$, $V_{TS2O} = 1V_{p-p}$	—	-65	—	dB
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V
	Input Bias Current	I_I	—		-100	—	100	nA
FMS FMSP [28] →FMSO [26]	Voltage Gain	G_V	—	$f = 500\text{Hz}$	9.5	10.0	10.5	V/V
	Frequency Characteristic	f_c	—		—	200	—	kHz
	Input Operating Voltage	V_I	—	GND reference	1.0	—	4.4	V
	Output Offset Voltage	V_{OS}	—	VR reference	-50	—	50	mV
	Total Harmonic Distortion	THD	—	$f = 500\text{Hz}$ $V_{FMSO} = 1V_{p-p}$	—	-65	—	dB
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V
	Input Bias Current	I_I	—		-100	—	100	nA

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DM DMEP [22] → DMEO [24]	Voltage Gain 1	G_{V1}	—	f = 1kHz DMEN = OPEN	1.9	2.0	2.1	V/V
	Voltage Gain 2	G_{V2}	—	DMEN - VR = 15k Ω	5.23	6.53	7.84	
	Frequency Characteristic	f_c	—		—	600	—	kHz
	Input Operating Voltage	V_I	—	GND reference	1.0	—	4.4	V
	Output Offset Voltage	V_{OS}	—	VR reference	-10	—	10	mV
	Total Harmonic Distortion	THD	—	f = 1kHz $V_{DMEO} = 1V_{p-p}$	—	-65	—	dB
	Upper Limit Output Voltage	V_{OH}	—	GND reference	3.8	—	—	V
	Lower Limit Output Voltage	V_{OL}	—	GND reference	—	—	0.5	V
DFCT	Voltage Gain	G_V	—	GND reference, DFIN→DFCT	0.86	0.91	0.95	V/V
	Supply Voltage	V_I	—	GND reference FHLD, THLD	0.0	—	5.0	V
	Attenuation Level	ATT	—	VR reference f = 1kHz, 4V $_{p-p}$	—	-40	—	dB
	On Voltage	V_{ON}	—	VR reference	-5	—	5	mV

OUTLINE DRAWING
QFP48-P-1014-0.80

Unit : mm



Weight : 0.83g (Typ.)